**What is claimed is:**

1. A solid-state imaging device having an A/D conversion circuit to which output signals from a plurality of circuit arrays are sequentially input, characterized in that

each of the circuit arrays comprises a photodetector, and a comparison circuit which receives a signal corresponding to an output from the photodetector and a monotonically increasing voltage, and outputs a coincidence signal representing a timing when the signal and voltage coincide,

said solid-state imaging device comprises a final coincidence determination circuit which receives a plurality of coincidence signals output from said comparison circuits and outputs a final coincidence signal representing a latest of timings represented by the coincidence signals, and

an A/D conversion range of the A/D conversion circuit is set in accordance with a value of the monotonically increasing voltage when the final coincidence signal is output.

2. A solid-state imaging device characterized by comprising:

N ($N \geqq 2$) photodetectors each of which outputs a signal current corresponding to an incident light intensity;

N integration circuits each of which is arranged in correspondence with one of said N photodetectors to integrate charges in correspondence with a signal current output from said photodetector and to output a signal voltage corresponding to an amount of the integrated charges;

N CDS circuits each of which is arranged in correspondence with one of said N integration circuits and has a first capacitor and amplifier sequentially inserted between an output terminal and an input terminal for receiving the signal voltage output from said integration circuit, second and third capacitors having the same capacitance value and parallelly inserted between an input and an output of said amplifier, and switch means for selecting one of said second and third capacitors to integrate a charge amount corresponding to an amount of a change in signal voltage;

N difference arithmetic circuits each of which is arranged in correspondence with one of said N CDS circuits to obtain a difference between the charge amounts integrated in said second and third capacitors of said CDS circuit and to output a difference signal voltage corresponding to the difference;

N S-H circuits each of which is arranged in correspondence with one of said N difference arithmetic

circuits to hold and output the difference signal voltage obtained by said difference arithmetic circuit;

a reference signal voltage generation circuit which outputs a reference signal voltage having a monotonically increasing value;

N comparison circuits each of which is arranged in correspondence with one of said N difference arithmetic circuits to compare a value of the difference signal voltage obtained by said difference arithmetic circuit with the value of the reference signal voltage output from said reference signal voltage generation circuit and to output a coincidence signal representing a timing when the values coincide;

a final coincidence determination circuit which receives coincidence signals output from said N comparison circuits and outputs a final coincidence signal representing a latest of timings represented by the coincidence signals;

a reference voltage hold circuit which receives the final coincidence signal output from said final coincidence determination circuit and the reference signal voltage output from said reference signal voltage generation circuit and holds and outputs the value of the reference signal voltage at the timing represented by the final coincidence signal; and

an A/D conversion circuit which sets an A/D

conversion range on the basis of the value of the reference signal voltage output from said reference voltage hold circuit, sequentially receives the difference signal voltages output from said N S-H circuits, converts each difference signal voltage into a digital signal, and outputs the digital signal.

3. A solid-state imaging device according to claim 2, characterized in that

said solid-state imaging device further comprises a timing control circuit which controls operations of said N integration circuits, said N CDS circuits, said N difference arithmetic circuits, said N S-H circuits, said reference signal voltage generation circuit, said N comparison circuits, said final coincidence determination circuit, said reference voltage hold circuit, and said A/D conversion circuit, and is used together with light projecting means for projecting spot light to an object,

said timing control circuit causing,

during a first period in which the spot light is being projected to the object by said light projecting means, said second capacitor of said CDS circuit to integrate the charge amount corresponding to the amount of the change in signal voltage output from said integration circuit when the spot light component and background light component become incident on said

photodetector,

during a second period in which the spot light is not projected to the object by said light projecting means, said third capacitor of said CDS circuit to integrate the charge amount corresponding to the amount of the change in signal voltage output from said integration circuit when the background light component becomes incident on said photodetector,

during a third period after the first and second periods, said difference arithmetic circuit to calculate the difference between the charge amounts integrated in said second and third capacitors of said CDS circuit and to output the difference signal voltage corresponding to the difference, and said S-H circuit to hold the difference signal voltage,

during a fourth period after the third period, said reference signal voltage generation circuit to output the reference signal voltage having the monotonically increasing value, said comparison circuit to output, on the basis of comparison between the values of the difference signal voltage and reference signal voltage, the coincidence signal representing the timing when the values coincide, said final coincidence determination circuit to output the final coincidence signal representing the latest of the timings represented by the coincidence signals, said reference

voltage hold circuit to hold the value of the reference signal voltage at the timing represented by the final coincidence signal, and said A/D conversion circuit to set the A/D conversion range on the basis of the held value of the reference signal voltage, and

during a fifth period after the fourth period, said A/D conversion circuit to sequentially receive the difference signal voltages output from said N S-H circuits, convert each difference signal voltage into a digital signal, and output the digital signal.

4. A distance measuring device characterized by comprising said solid-state imaging device of claim 2, and a light source which supplies light to be incident on said solid-state image sensing element, wherein said solid-state imaging device and said light source are fixed on a single circuit board.